

ATS 24232

N72-21209

NASA SP-5949 (01)

TECHNOLOGY UTILIZATION

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DIGITAL CIRCUITS FOR COMPUTER  
APPLICATIONS

A COMPILATION



NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

## Foreword

The National Aeronautics and Space Administration and the Atomic Energy Commission have established a Technology Utilization Program for the dissemination of information on technological developments which have potential utility outside the aerospace community. By encouraging multiple application of the results of their research and development, NASA and AEC earn for the public an increased return on the investment in aerospace research and development programs.

The innovations in this updated series of compilations dealing with electronic technology represent a carefully selected collection of digital circuits which have direct application in computer oriented systems.

Throughout the years, as the NASA space programs grew in size and complexity, there also was a commensurate increase in the use of electronics technology. Almost invariably the role of digital computers has played a dominant role, both in the test and evaluation phase and in the actual implementation of the spaceborne hardware. These circuits represent a mere sampling of the immense volume of items that are available through the NASA TU program. In general, the circuits have been selected as representative items of each section and have been included on their merits of having universal applications in digital computers and digital data processing systems. As such, they should have wide appeal to the professional engineer and scientist who encounter the fundamentals of digital techniques in their daily activities.

Additional technical information on individual devices and techniques can be requested by circling the appropriate number on the Reader Service Card included in this compilation.

Unless otherwise stated, NASA and AEC contemplate no patent action on the technology described.

We appreciate comment by readers and welcome hearing about the relevance and utility of the information in this compilation.

Jeffrey T. Hamilton, Director  
Technology Utilization Office  
National Aeronautics and Space Administration

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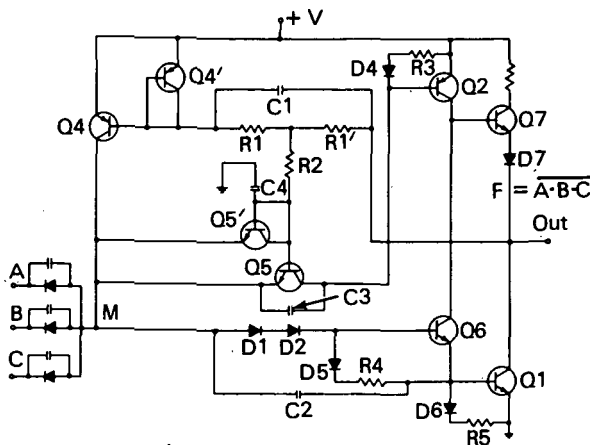
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# Section 1. Digital Logic Circuits

## LOW POWER NAND GATE

Low power operation creates many problems in integrated circuit design. The rationale for achieving low power operation is the optimization of the possible trade-off conditions. If the



power dissipation of a circuit is to be reduced, either the voltage or the current, or both, must be reduced. In any case, compromises must be made in the circuit gain, speed, and noise immunity.

The circuit shown in the figure uses a complementary pnp transistor, Q2, as the load resistor to reduce the switching time and the steady state dc current, and to allow for a lower supply voltage.

An auxiliary transistor, Q5, is connected between the common node M and the base of Q2. When all the inputs are at the "1" level, the base of Q5 assumes a potential lower than the emitter,

and Q5 is cut off. When any one of the inputs is at "0" level, the node potential at M drops below that at the base of Q5 and turns on Q5, causing the base current of Q2 to flow. Q5 also serves as the initiator for starting the regenerative pnp switching action when all the inputs are at the "1" state. Once point M becomes unclamped by the input diode, the forward biased junctions of Q4 and Q5 force a current to flow into the base of Q1 through the level setting diodes, and regeneration takes place.

Capacitors C1, C2, and C3 provide a low impedance charging path for the charging currents in order to decrease the turn-off time. The resistor-diode combinations, shunting the base emitters of Q2, Q6, and Q1, maintain constant current gain and provide bleedoff paths for leakage current,  $I_{CBO}$ . The collector of Q6 is connected to the base of Q7 to speed up the turnoff of Q7; Q2, aided by Q7, provides a high output current when the output is at the "1" state.

Conventional integrated circuit processing is used to fabricate the gates, with the one addition of thin-film tantalum resistors deposited on the surface of the die.

Source: H. C. Lin of  
Westinghouse Electric Corp.  
under contract to  
Marshall Space Flight Center  
(MFS-14487)

Circle 1 on Reader Service Card.

## LOAD SWITCHING AND LOGIC DESIGN CRITERIA

A discussion of design criteria for improved load switching techniques is contained in this electrical system analysis report. Advanced logic design for application to complex elec-

trical systems is presented and the circuit analysis for the developed hardware is outlined. The report is the outcome of a study of advanced techniques for synthesizing the operations of

large electrical systems. In review, the process of system synthesis was accomplished by giving consideration to the various electrical system techniques and their ability to accomplish the program objectives in the following areas: (1) system layout; (2) power sources; (3) power control; (4) packaging; and (5) the distribution system.

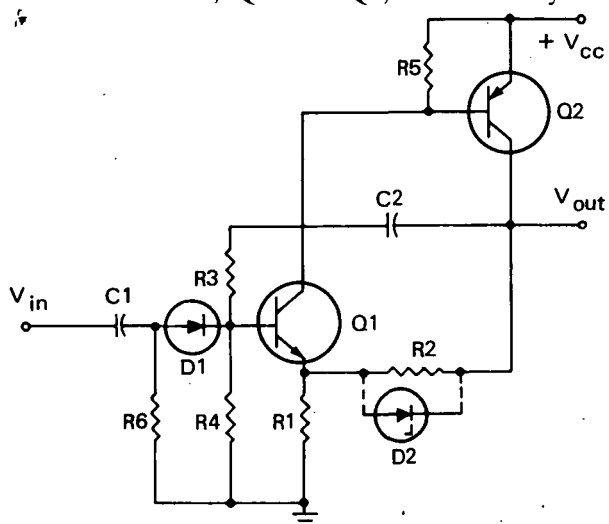
The conclusions derived from the review can readily be applied to such analogous systems as electrical power distribution equipment.

Source: The Boeing Company  
under contract to  
Marshall Space Flight Center  
(MFS-13884)

*Circle 2 on Reader Service Card.*

### COMPLEMENTARY MONOSTABLE CIRCUITS ACHIEVE LOW POWER DRAIN AND HIGH RELIABILITY

A complementary monostable multivibrator has virtually no power drain in standby operation. The transistors, Q1 and Q2, are normally off



in the absence of a biasing voltage. When a positive trigger pulse is applied to the input coupling network (C1, R6, D1), both transistors turn on and positive regeneration occurs. As C2 begins to charge, the base voltage of Q1 decreases exponentially until Q2 comes out of saturation. Negative regeneration then occurs and the circuit turns off. The base voltage required to remove Q2 from saturation is approximately the supply voltage divided by the forward gain.

The output pulse width can be varied by changing R2. Temperature compensation is obtained by inserting the proper thermistor in series with R1.

Source: L. L. Kleinberg and C. Lavigne  
Goddard Space Flight Center  
(GSC-00433)

*No further documentation is available.*

### SWITCHING CIRCUITS WITH FAST RESPONSE AND LOW POWER DRAIN

These logic circuits have response times less than 10 nanoseconds and drain only a few milliwatts of power. They include AND and NAND

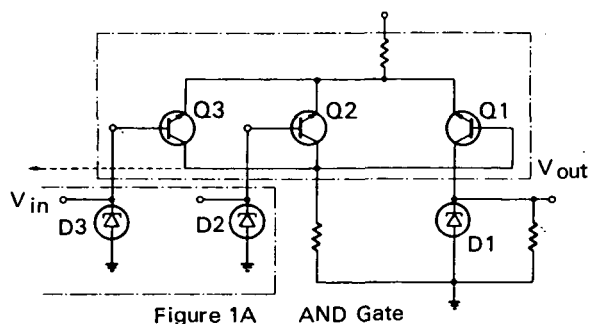


Figure 1A AND Gate

gates with the associated monostables, bistables, delays, and oscillators. The basic circuits perform all logic functions and can be used in a variety of digital-data-processing systems.

A typical AND gate is shown in Fig. 1A where the input signals are derived across tunnel diodes D1 and D3 and applied to transistors Q2 and Q3. The output is taken across D1 which is connected to the voltage source through Q1.

In the NAND gate (Fig. 1B) the input signals are taken across tunnel diodes D5 and D6 and applied to input transistors Q5 and Q6. The output is taken across D4.

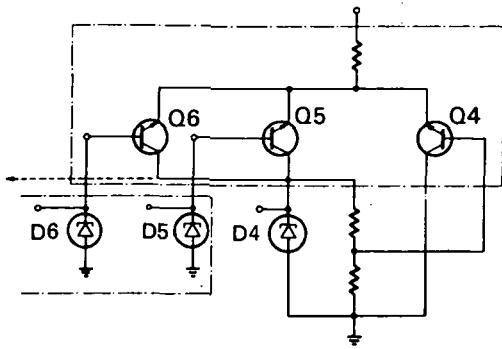


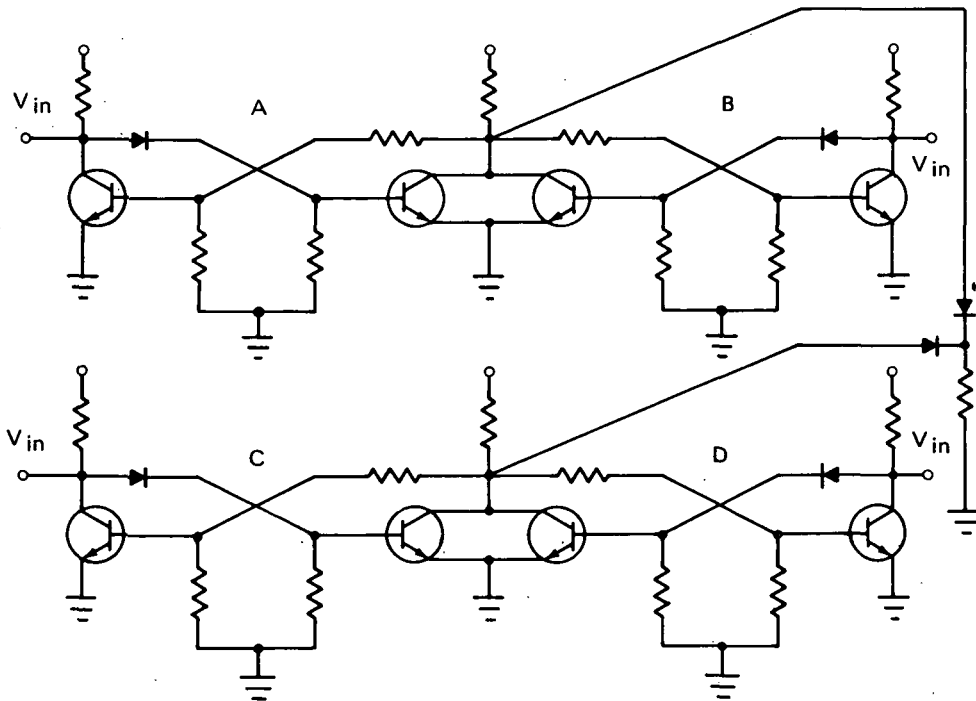
Figure 1B NAND Gate

The logic circuits have low output impedance and high input impedance enabling them to be used in a logic chain without need of coupling elements or buffer amplifiers. Moreover the circuits operate from a single-level voltage source and have a substantially constant current drain, so that noise spikes and the need for a multi-level-voltage source are eliminated.

Source: C. A. Cancro  
Goddard Space Flight Center  
(GSC-10878)

Circle 3 on Reader Service Card.

### LOGICALLY REDUNDANT FLIP-FLOP



Because of the limited reliability of electronic circuit components, quite often conventional circuitry cannot fulfill a given reliability requirement that has been imposed by a particular system. The only course left open to the circuit designer is to choose some form of redundancy. The figure illustrates a flip-flop where logic redundancy is employed.

A, B, C, and D are the common transistor flip-flops. The AND and OR gates are implemented with passive components, and there-

fore, are of high reliability. Since only the flip-flops use transistors, they represent the weak link in the system. However, because of the logic redundancy, any flip-flop may fail and the circuit will still yield a true answer, e.g., assuming A to fail in the zero state, the output of the first AND gate is  $A \cdot B = 0 \cdot B$ . Hence, the output of the OR gate is CD; which is a true answer. If A is assumed to fail in the 1 state, the output of the first AND gate is  $A \cdot B = 1 \cdot B = B$ , and the output of the OR gate

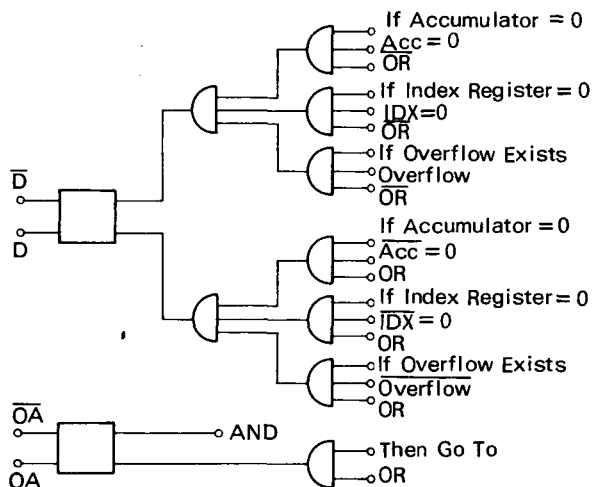
$B+CD$ , which is a true answer. The most efficient method of implementing this logic diagram is shown in the figure. Here, the AND gates are constructed by merely paralleling the 1-output sides of the flip-flops. The OR gate is a conventional diode gate.

Source: Kollsman Instrument Corp.  
under contract to  
Goddard Space Flight Center  
(GSC-90550)

*Circle 4 on Reader Service Card.*

## LOGIC CIRCUIT AIDS IN REDUCING PROGRAMMING ERRORS

A unique method for applications with general purpose computers has been developed for combining many conditions before performing a conditional transfer. The technique is very



flexible, requires simple logic circuitry and is especially adaptable for computers where programs are written using complete sentences.

The logic circuit implementation of this technique uses a series of flip-flops and gates. Special test instructions are used to set the D flip-flop according to other conditions within the computer. A conditional transfer then senses

the state of the D flip-flop and will execute the transfer if D is set. In order to combine various test conditions in some logical form, a second flip-flop, OA, is used to combine, by either an OR (OA set) or AND (OA reset), any number of test conditions into the D flip-flop. The combination of OA and D flip-flops is then used to produce the desired combination of transfer conditions for the computer. When the conditional transfer instruction occurs, the D flip-flop will reset and the OA flip-flop will set, thus destroying the result of the previous tests and setting up the flip-flops for the next transfer and set of test conditions.

The major advantage of this method is that direct machine execution of statements in a parenthesis-free English language is supplied to the computer. As such, it provides the programmer with a powerful tool, simplified for easy use, that shortens the time required to complete a task and eliminates sources of confusion and error.

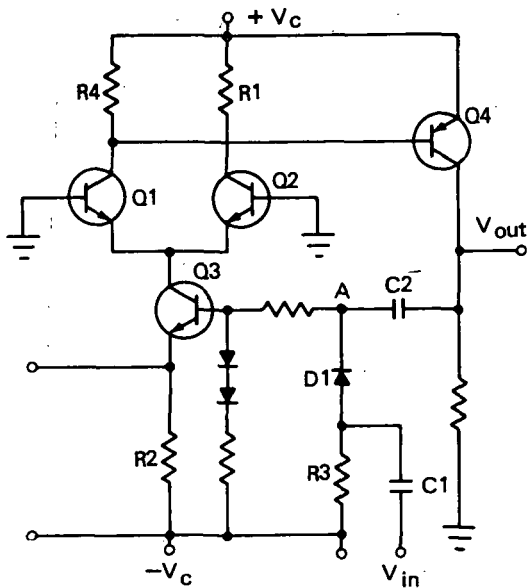
Source: D. K. Sloper of  
Westinghouse Electric Corp.  
under contract to  
Goddard Space Flight Center  
(GSC-10740)

*Circle 5 on Reader Service Card.*

## LOW-POWER INTEGRATED CIRCUIT FOR COMPUTER APPLICATIONS

This monostable integrated circuit has no power dissipation in the standby state. It should find general application for signal control and conditioning. The basic circuit consists of transistors Q1, Q2, and Q3 connected in a differential

amplifier configuration. Q3 is a constant current source, whose current is determined by the dc potential at terminal A and the value of R2. With no dc potential at terminal A, no current flows and Q1 and Q2 are nonconducting. When



a positive trigger pulse is applied to the coupling network (C1, R3, and D1), current flows through Q3 and the voltage drop across its load resistor turns on Q4; the positive going potential at the collector of Q4 is fed back through C2 to the base of Q3, driving it even harder. The circuit is regenerative and Q4 quickly goes into saturation.

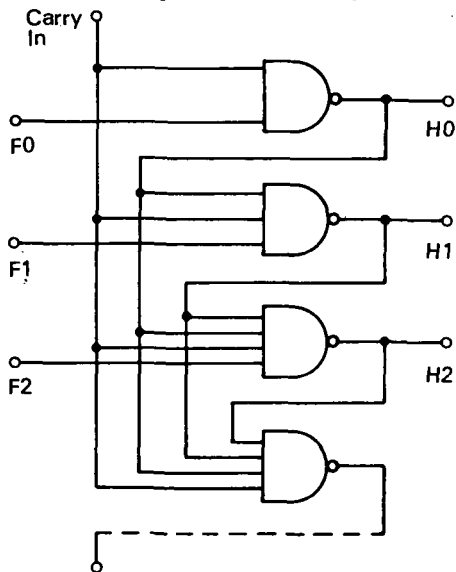
When Q4 comes out of saturation, regeneration in the negative direction takes place and Q3 quickly cuts off, turning off Q1, Q2, and Q4. The system now dissipates no power until the next trigger pulse is applied.

Source: L. L. Kleinberg  
Goddard Space Flight Center  
(GSC-10082)

*No further documentation is available.*

### PRIORITY LOGIC

The priority gates (see fig.) form the basis of a method to determine the lowest order input terminal which has a high input. The "H" output corresponding to this input will be low, and all other "H" outputs will be high. With the



initial assumption that the ENABLE input is low, and remains low until all "F" inputs have become either valid or low, the carry inputs to all 8-bit priority gates are caused to be high. One prime feature of the circuit design is to minimize the delay between the positive edge of the ENABLE input and the time that all "H" outputs (except the first selected one) are high.

The binary address of the first high "F" input can be easily encoded from the "H" outputs; the least significant bit of the address is the NAND function of all odd-numbered "H" outputs and the second least significant bit is the NAND function of every other pair of "H" outputs, i.e.  $H2 \cdot H3 \cdot H6 \cdot H7$ . This logic can be implemented with off-the-shelf high-speed TTL logic elements.

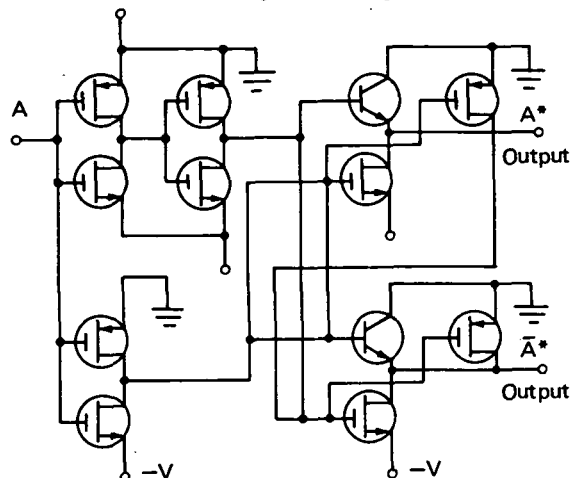
Source: American Micro-Systems, Inc.  
under contract to  
Marshall Space Flight Center  
(MFS-21184)

*No further documentation is available.*



### LOW-POWER COMPLEMENTARY BIPOLAR BUFFER

An inverting/non-inverting buffer shown in the figure easily drives loads, with capacitances as high as 150 pF, at high switching speeds and with a minimal dissipation of power. The tech-



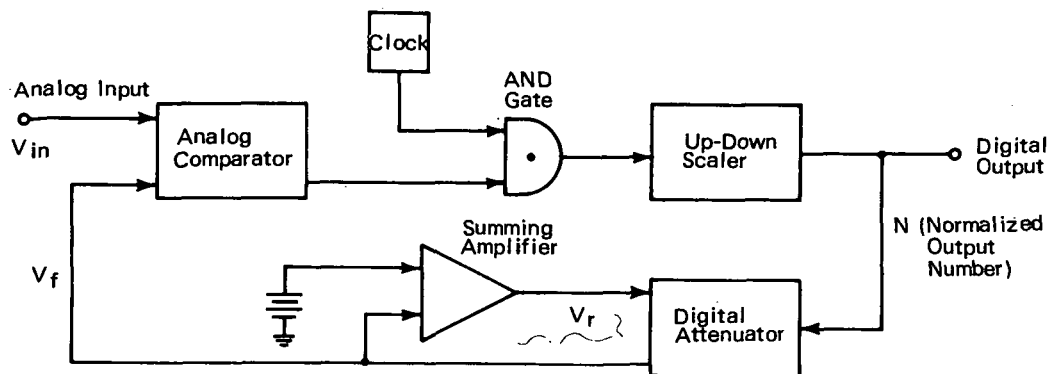
nique of alternately turning one of the output transistors off during switching (allowing a time delay), and then turning the alternate output transistor on, reduces current consumption significantly for switching applications. The circuit has special merit for driving arrays of capacitive integrators. The waveforms for the devices used in the circuit were computed from a special FORTRAN IV program which used the standard saturated and unsaturated current equations, and integration and differentiation subroutines to solve for the output voltages and currents.

Source: General Instrument Corp.  
under contract to  
Marshall Space Flight Center  
(MFS-20949)

Circle 6 on Reader Service Card.

## Section 2. Analog-to-Digital Converters

### NONLINEAR FEEDBACK REDUCES ANALOG-TO-DIGITAL CONVERTER ERROR



The accuracy of a conventional, linear analog-to-digital converter is limited at low input voltage levels due to the inherent quantization error, i.e., an inability to measure increments smaller than the least significant digit. This nonlinear analog-to-digital converter measures the level of an analog input and con-

tinuously adjusts the scale sensitivity of the digital readout to attain an effective increase in accuracy. As the output level decreases, the scale sensitivity increases to retain a more nearly constant accuracy as expressed in percentage of reading, thus permitting the acquisition of more accurate low-level data.

In order to obtain the nonlinearity necessary for scale adjustment, an accurate nonlinearity function is placed in the conventional feedback path. This is done in the feedback elements consisting of the summing amplifier, reference voltage, and digital attenuator. These elements are capable of a high degree of accuracy as compared to other possible nonlinear elements.

The nonlinear analog-to-digital converter (shown in the figure) consists of six basic subsystems: an analog comparator, a clock and control gate, an updown scaler, a digital attenuator, a summing amplifier, and a fixed voltage source.

The analog voltage to be sampled is fed into the analog comparator which produces an output if there is any difference between  $V_{in}$  and  $V_f$  (the feedback voltage). Any output from the comparator turns the AND gate on and allows the clock signal to be fed to the up-down scaler. The up-down scaler produces the output in digital form.

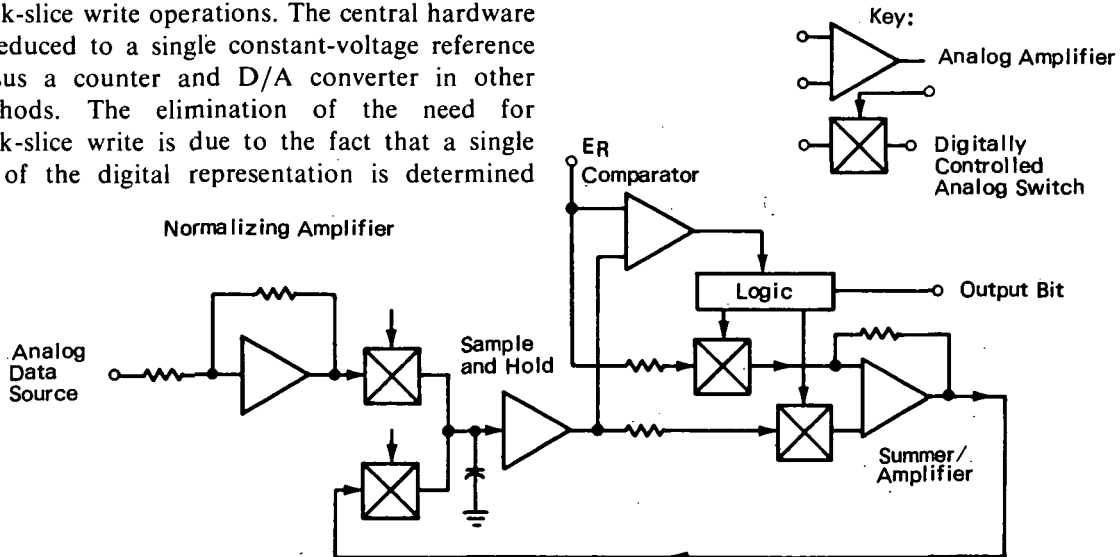
Source: R. M. Munoz  
Ames Research Center  
(ARC-00046)

*Circle 7 on Reader Service Card.*

## ANALOG-TO-DIGITAL CONVERTER USES SEQUENTIAL APPROXIMATION TECHNIQUE

In addition to having a faster conversion rate, the sequential approximation of performing analog-to-digital conversion also minimizes the amount of central hardware, and eliminates the work-slice write operations. The central hardware is reduced to a single constant-voltage reference versus a counter and D/A converter in other methods. The elimination of the need for work-slice write is due to the fact that a single bit of the digital representation is determined

of these functions. The analog input is normalized, sampled, and stored in a holding circuit. It is then compared with the reference voltage ( $E_R$ ) which is set at one-half the magnitude of



for all analog inputs during each step of the conversion operation. Thus the bit-slice write operation can be used to transfer one bit-at-a-time of the digital number to the strand memory.

The sequential approximation method outlined in the block diagram represents the function being performed and not the actual circuits, since there are several ways of performing many

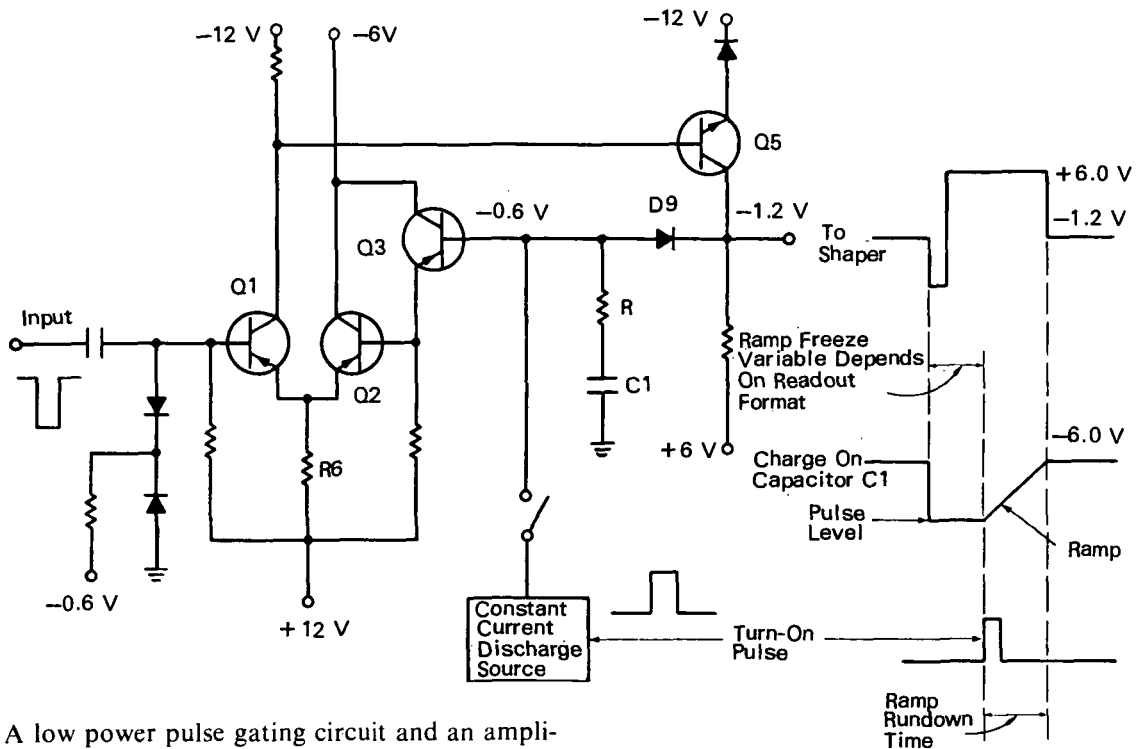
the largest voltage to be converted. For all strands in which the input voltage is greater than or equal to  $E_R$ , the output bit is made a "1", the reference voltage  $E_R$  is subtracted from the input voltage, and this difference voltage is then multiplied by two. For all strands in which the input voltage is less than  $E_R$ , the output bit is made a "0" and the input voltage is multi-

plied by two. The output of the "doubling" amplifier is then stored in the input holding circuit in place of the input from the data source. This procedure is repeated until a sufficient number of bits (the required precision) is obtained.

Source: G. J. Prom, C. W. Hastings and H. R. Holt of Honeywell, Inc. under contract to Electronics Research Center (ERC-10007)

*Circle 8 on Reader Service Card.*

### LOW-POWER ANALOG-TO-DIGITAL CONVERTER MEASURES NANOSECOND PULSE WIDTHS



A low power pulse gating circuit and an amplitude-to-time converter responds to pulses as short as 200 nanoseconds. Linear operating characteristics are achieved over a range of input pulse amplitudes from 5 mV to 5.12 V. This type of signal conditioner can be used to process analog information prior to its entry into a computerized data system.

In operation, a pulse is accepted by a linear gate and is entered to the amplitude-to-time converter which converts the pulse amplitude variations to time-width variations. The converter circuit, shown in the figure, is a variation of a pulse stretcher, wherein a temperature-stable, silver-mica capacitor C1 is charged to the peak

pulse amplitude through a series transistor and diode, and is then permitted to discharge, at a controlled rate through a constant current source.

The input pulse to be measured appears on one side of the comparator (an emitter-coupled pair consisting of Q1 and Q2) that supplies drive to Q5 and charges the capacitor through diode D9. The loop returns this capacitor voltage to the opposite side of the comparator in a common-mode nulling arrangement. With zero charge on the capacitor a large error voltage is developed at the collector of Q1 and the capacitor charges rapidly to the peak amplitude of the pulse,

bringing the error voltage to zero. Q5 ceases conducting and D9 becomes reverse-biased as the collector of Q5 rises to +6 volts.

The capacitor retains this amplitude-proportional charge until a predetermined time, when a turn-on pulse, fed into the discharge switch, initiates the linear ramp discharge. At the end of the ramp rundown, Q5 and D9 recover rapidly from cut-off and the collector of Q5 reverts to a negative voltage. Thus, two well-defined, time-domain points are available for generating a

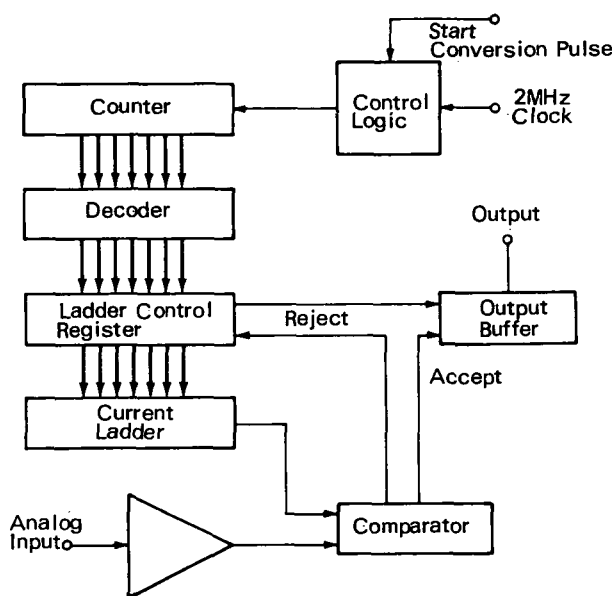
square wave, the width of the generated pulse being pulse-amplitude dependent and suitable for gating a succeeding oscillator circuit. The gated pulse train from the oscillator represents the digital conversion of the analog information contained in the input pulse.

Source: C. Cancro and N. Garrahan  
Goddard Space Flight Center  
(GSC-10337)

*Circle 9 on Reader Service Card.*

### SMALL, LOW-POWER ANALOG-TO-DIGITAL CONVERTER

The converter can be used in any digital system in which it is necessary to convert an analog voltage into a serial digital signal (and 8-bit accuracy is acceptable) such as automated produc-



tion or process control systems. With further development, the converter could be improved to operate at a higher speed and with greater accuracy.

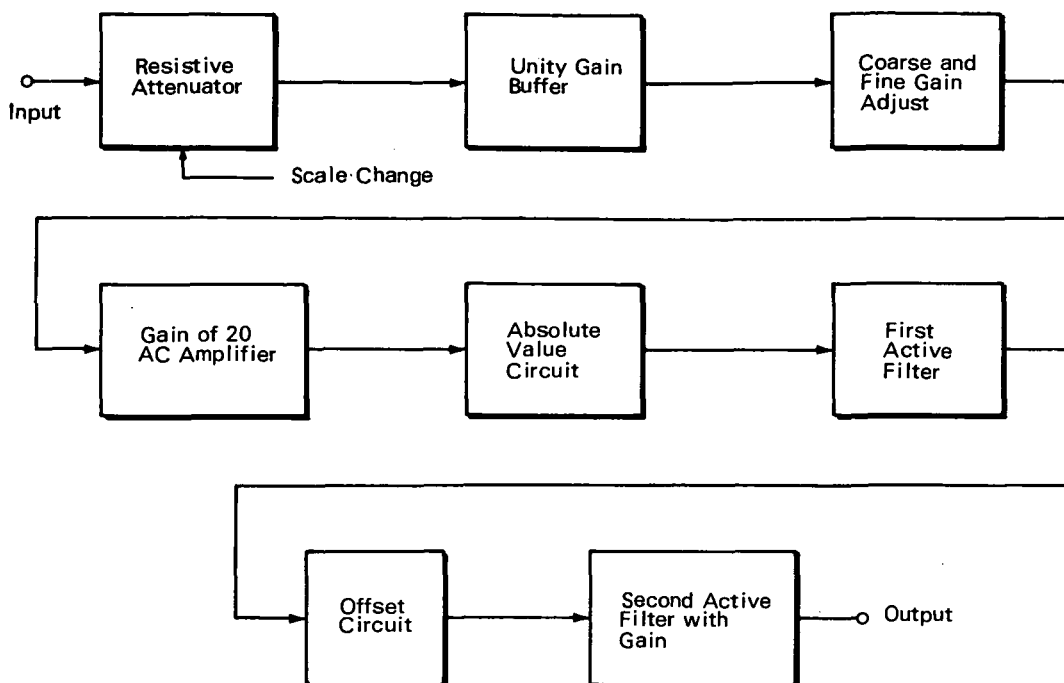
Total power consumption is less than 840 mW. The successive approximation method of A-to-D conversion generates the digital output with bit rate of 1 MHz and a maximum conversion rate of 125 kHz. Overall volume of the converter, packaged in four potted modules, is approximately 5 cc.

Operation of the converter begins with a start conversion pulse that resets the control logic, counter, and ladder control register. The most significant bit in the ladder control register is set (by a specific output from the decoder) to switch the most significant current from the current ladder to the comparator summing line. After the end of the start conversion pulse, the bit 1 current is compared with the current derived from the analog input. If the summed ladder current is smaller than the analog current, the bit is retained; if it is larger, a dump pulse is generated to reset the appropriate control register flip-flop. When the flip-flop resets, the corresponding ladder current is switched off the summing line. At the end of the bit time (1 msec), the counter advances a single count. This advance switches in the next smaller bit, the comparison is made after a 750 ns settling time, and the bit is then either accepted or rejected. The procedure is repeated until all 8 bits have been compared. The control logic then resets register bits 2 through 8 and maintains the counter in bit-time zero until the next start conversion pulse is received. Simultaneously with each comparison, the output flip-flop is set if the bit is accepted and reset if the bit is rejected.

Source: D. H. Fullerton and R. D. Dunn of  
The Boeing Company  
under contract to  
Marshall Space Flight Center  
(MFS-13954)

*Circle 10 on Reader Service Card.*

### PRECISION AC-TO-DC CONVERTER HAS EXPANDED SCALE OPERATION



A highly accurate ac-to-dc converter responds to the average value of a full wave rectified ac signal over a frequency bandwidth from 50 Hz to 10 kHz. The circuit is constructed entirely of solid state components and provides for an expanded scale operation. The converter has general application as a signal conditioner for complex computer-aided test operations. An improved absolute-value circuit performs the rectification process and after this process the circuit becomes average responding.

Important design parameters include: (1) over-

all accuracy on any range is 0.5% of full scale output; (2) full scale dc output is adjustable from 0 to 10 V; (3) input impedance is greater than 560 k $\Omega$ ; and (4) output noise is less than 8 mV peak-to-peak.

Source: M. A. Smither and D. N. Moss of General Electric Co. under contract to NASA Headquarters (HQN-10510)

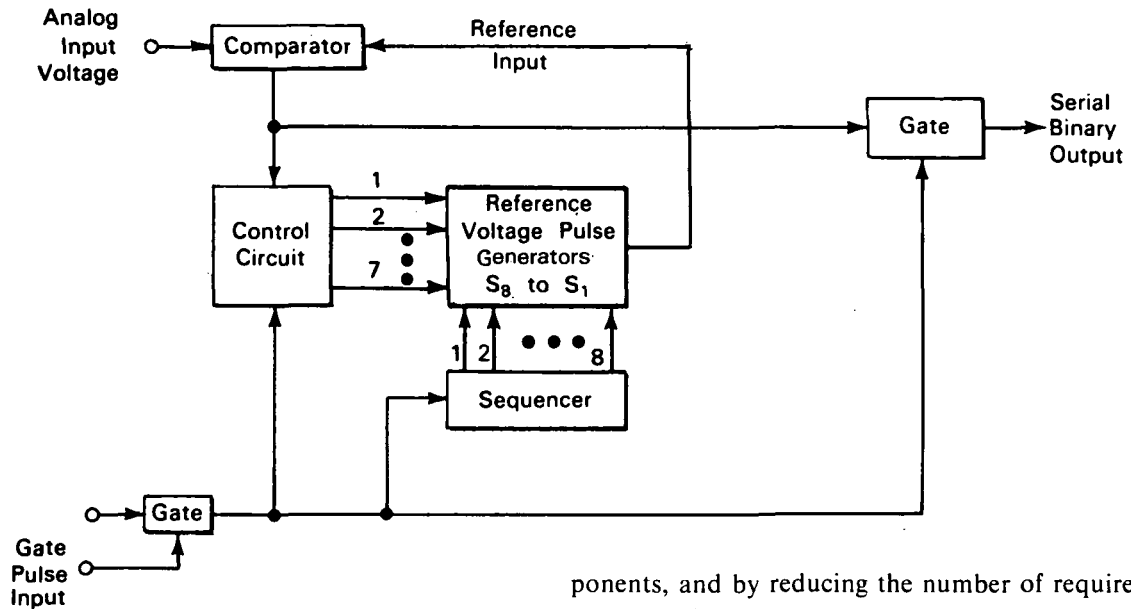
Circle 11 on Reader Service Card.

### ANALOG-TO-DIGITAL CONVERTER HAS INCREASED RELIABILITY AND REDUCED POWER CONSUMPTION

An eight-bit analog-to-digital converter operates in a pulse mode that minimizes power consumption and increases reliability.

Eight reference 400-Hz clock pulses (applied to the memory control circuit, the sequencer, and the output gate) control and time the formation of the binary number. The output from each reference pulse generator is applied to the comparator, where the amplitude of the reference voltage pulse is compared to the amplitude of

the analog voltage input. If the analog voltage amplitude is greater, a "1" is formed at the binary output, and the memory control circuit triggers that particular reference pulse generator for the remainder of the eight clock pulses. That particular reference output is therefore summed with each of the remaining reference pulse outputs as they are sequentially triggered by succeeding clock pulses, i.e.,  $S_8 + S_7$ ,  $S_8 + S_6$ , . . .  $S_8 + S_1$ . A "0" is formed at the binary



output when the analog amplitude is less than the reference amplitude.

The memory control circuit uses a nonlinear core transformer combined with a linear core transformer in a one-shot blocking oscillator circuit. The nonlinear core transformer performs as the memory element and the blocking oscillator acts as a delay element which keeps the nonlinear core transformer in the proper state of operation. The use of magnetic core components increases reliability, both through the inherent reliability of magnetic core com-

ponents, and by reducing the number of required components.

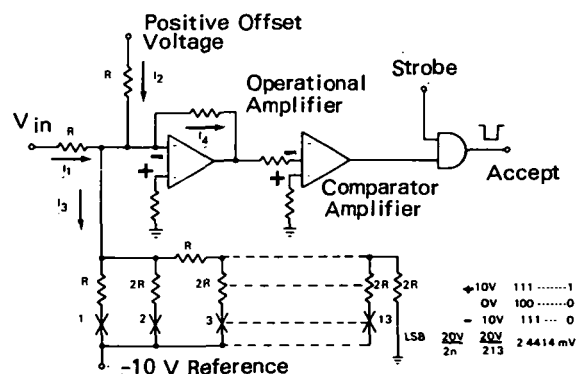
The reference pulse generators are blocking oscillators with nonlinear transformer cores. Average power consumption is reduced by the use of the blocking oscillators (which are in a cutoff state part of the time) instead of flip-flops which always have one component conducting.

Source: J. C. Thornwall  
Goddard Space Flight Center  
(GSC-00246)

Circle 12 on Reader Service Card.

## HIGHLY LINEAR, SENSITIVE ANALOG-TO-DIGITAL CONVERTER

The analog-to-digital (A/D) converter shown in the schematic converts a 10 volt input signal into a 13 bit digital output. The converter has a least significant bit (LSB) weight of 2.44 mV, and has a nonlinearity of 0.0075 percent over the temperature range of 273 to 343 K. Other advantages of the converter, in addition to its high sensitivity and linearity, include: low quantizing error (1/2 of the LSB, or 1.2207 mV), high resistance to mechanical shock and vibration loads; and temporary data storage capabilities. It has a moderate conversion speed of 20 microseconds per bit, but has been operated equally well at a 10 microsecond bit rate.



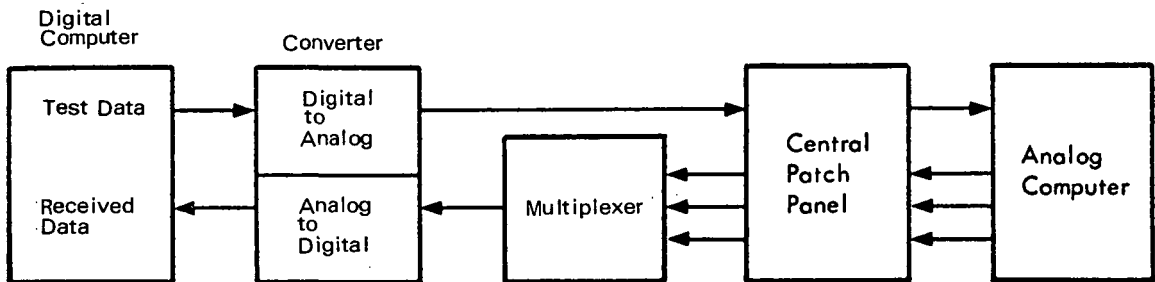
The A/D converter incorporates a very stable, regulated  $-10$  volt ladder reference supply and a positive offset voltage supply. When a voltage appears at the input terminal, the most significant bit (MSB) of the ladder is switched from ground to the  $-10$  volt reference supply. If the sum of the input current ( $I_1$ ) is greater than the current ( $I_3$ ) furnished by the MSB, the output of the operational amplifier goes negative, so that the feedback current ( $I_4$ ) balances the currents at the summing junction. The output of the comparator, which is operated open loop, thus goes positive. At the end of the 20 microsecond comparison time, a strobe pulse is generated and an "accept" pulse sets a flip-flop to hold on the MSB switch. The second bit is then tried. If

the sum of the input and offset currents is less than the sum of the two MSB currents, the second bit will be rejected. The cycle continues until all 13 bits have been tried and accepted (or rejected). The digital data are stored in the memory flip-flops which control the ladder switches. These data are available for use until the flip-flops are cleared prior to another conversion.

Source: W. R. Finley and J. Cox of  
Gulton Industries, Inc.  
under contract to  
Manned Spacecraft Center  
(MSC-13110)

*No further documentation is available.*

### SELF-CHECK TECHNIQUE FOR HYBRID COMPUTER SYSTEM



A computerized technique automatically checks the conversion interchange of analog to digital (or digital to analog) data in a hybrid computer system. In the simplified diagram of the system shown in the figure, the test data from the digital computer are converted from known digital data to a single analog data channel. The output of the digital computer is a binary word representing a 2-V signal. The D/A converter changes the binary word into an analog dc voltage value representing a 2-V value.

The converted signal is routed through a central patch panel and is applied as an input to the analog computer. The analog computer places the input 2-Vdc signal on one, (or several output circuits) depending on the circuit program, or complexity of the self-check. The dc voltage, representing the original 2-V digital

signal, is now routed back from the analog computer over 3 incoming separate paths. The laboratory multiplexer sequentially samples each of the three incoming analog signals and routes them simultaneously on a single channel. The incoming data in analog form are converted back to digital data by the A/D converter and routed back to the digital computer. If the incoming digital signal is a precise 2-V binary word, the received data are identical to the original test data and the system is in perfect calibration.

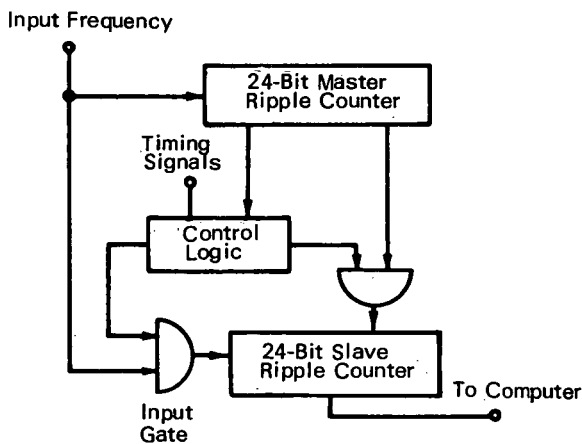
Source: J. Browning of  
IBM Corp.  
under contract to  
Marshall Space Flight Center  
(MFS-14237)

*Circle 13 on Reader Service Card.*

## Section 3. Counters and Shift Registers

### DIGITAL FREQUENCY COUNTER PERMITS READOUT WITHOUT DISTURBING COUNTING PROCESS

A digital frequency counter, incorporating a master counter and a slave counter with novel logic interconnections, reads accurately at one-second intervals without interrupting or disturbing



the counting process. The counter can monitor frequencies from dc to 50 MHz in steps of 0.01 Hz.

Two 24-bit ripple counters (a master and a slave) count the input frequency; in addition, the slave counter can be synchronized to the master counter or disconnected from the input frequency by the control logic.

Both the signal from the input gate and the synchronizing signals from the master counter are connected to the slave counter. The synchronizing signals are fed directly into the inputs of the slave counter flip-flops, which are represented by the 24-bit gating structure. When a carry

ripple is propagating through the master counter, the slave counter is in an indeterminate state because of possible interference between the synchronizing signals and the slave internal ripple signals. When no ripple is present in the master counter, the state of the slave counter is exactly that of the master counter. The control logic disconnects the synchronizing signals from the slave counter at a time when no ripple is in the master counter (since the ripple in the slave counter occurs at the same time as the ripple in the master counter). The condition of no-ripple exists when the first 4 least-significant-bit positions of the master counter are equal to 1, indicating that 15 counts of the input frequency have occurred after the previous major carry bit has been propagated. Sufficient time has thus been allowed for all carries to have been completely propagated. At this time both counters are counting the same signal and contain the same count, but otherwise are completely independent of each other. When the instantaneous count value is desired, the input signal is disconnected from the slave counter. After any carry ripples have finished propagating in the slave counter, the individual slave counter flip-flops can then be read by a computer.

Source: R. Winkelstein  
Jet Propulsion Laboratory  
(JPL-00906)

*Circle 14 on Reader Service Card.*

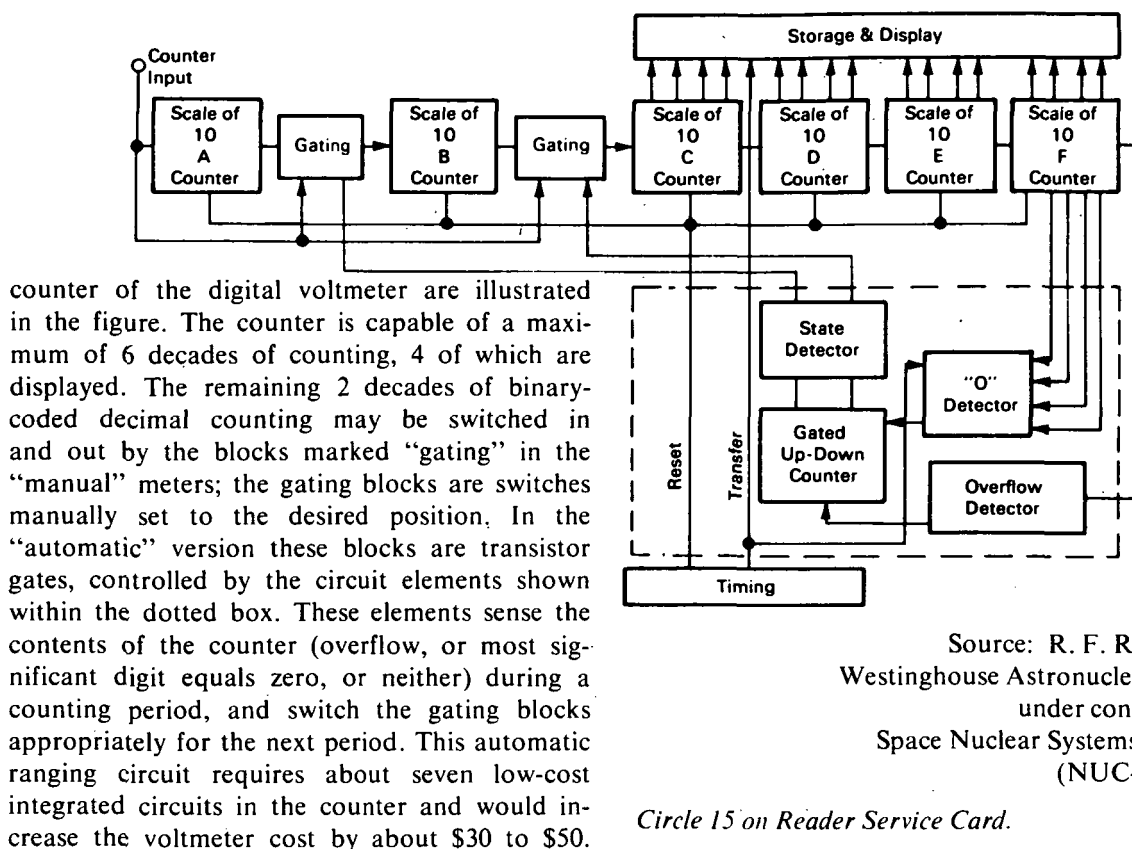
### AUTOMATIC RANGING FOR DIGITAL VOLTMETERS AND FREQUENCY COUNTERS

A simple automatic ranging circuit can be incorporated, at very low cost, into voltage-to-frequency digital voltmeters and frequency count-

ers. Extra decades are switched into and out of the counter during the previous counting period.

The counting path and display section in the

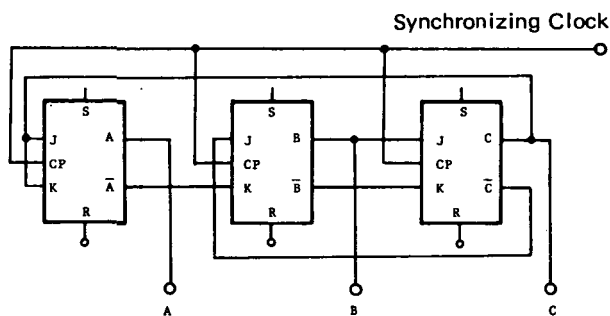




Source: R. F. Roller of  
Westinghouse Astronuclear Lab.  
under contract to  
Space Nuclear Systems Office  
(NUC-10240)

Circle 15 on Reader Service Card.

### SYNCHRONOUS MODULO 8 COUNTER REQUIRES NO GATES



The novel implementation in this circuit is a synchronous modulo 8 counter, containing only 3 J-K universal flip-flops and requiring no gates. For clarity, the J-K flip-flops behave in the following manner: if  $J=K=0$ , the clock pulse CP will have no effect; if  $J=1$  and  $K=0$ , the next CP will set the flip-flop; if  $J=0$  and  $K=1$ , the next CP will reset the flip-flop; and, if  $J=K=1$ , the next CP will complement the present state

A	B	C	JA	KA	JB	KB	JC	KC
0	0	0	0 NE	0	1 TOG	1	0 CLR	1
0	1	0	0 NE	0	1 TOG	1	1 SET	0
0	0	1	1 TOG	1	0 CLR	1	0 CLR	1
1	0	0	0 NE	0	1 SET	0	0 CLR	1
1	1	0	0 NE	0	1 SET	0	1 SET	0
1	1	1	1 TOG	1	0 NE	0	1 SET	0
0	1	1	1 TOG	1	0 CLR	1	1 SET	0
1	0	1	1 TOG	1	0 NE	0	0 CLR	1

Truth Table

TOG = toggle  
NE = no effect  
CLR = clear  
SET = set

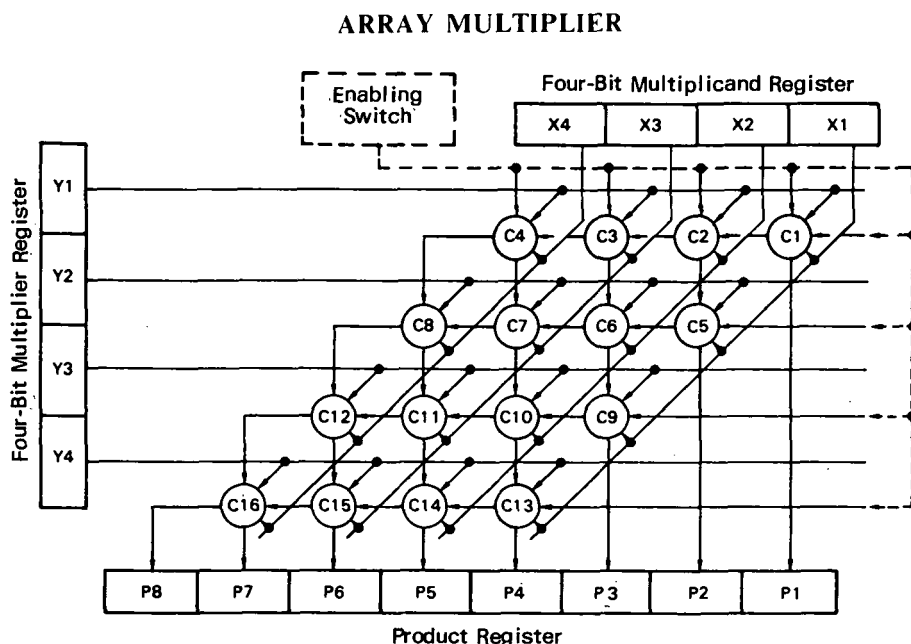
(toggle) of the flip-flop. Such flip-flops are readily available commercially in TTL lines (usually two per 14-lead integrated circuit package).

The solution is obtained by wiring the three flip-flops according to the following set of equations:  $JA=C$ ,  $KA=C$ ,  $JB=\bar{C}$ ,  $KB=\bar{A}$ ,  $JC=B$ ,  $KC=\bar{B}$ , as is shown in the diagram.

The truth table presents the 8 sequential output states at A, B, and C and illustrates how the specified connections generate the sequence, e.g., in the state 010, the A flip-flop would not be affected, the B flip-flop would be toggled, and C flip-flop would be set, giving the state 001 on the next line of the table.

Source: W. A. Lushbaugh of  
Caltech/JPL  
under contract to  
NASA Pasadena Office  
(NPO-11086)

Circle 16 on Reader Service Card.



A digital array multiplier consisting of identical digital adder cells in a repetitive planar configuration has general application in digital data systems.

Sixteen logic cells (C1-C16) are arranged in 4 rows of 4 bits each, and correspond to the partial products as dictated by the corresponding multiplier bits (see fig.). In the array network, the 4-bit multiplicand is stored in the uppermost register, the 4-bit multiplier is stored in the register at the left, and the product is stored in the 8-bit register at the bottom.

Physically, each bit of the multiplicand (X1, X2, X3, X4) is coupled to a cell element of the

partial product row for all rows in the corresponding bit position: X1 is coupled to cells C1, C5, C9, and C13. Each multiplier bit (Y1, Y2, Y3, Y4) is coupled to all cell elements of the corresponding partial product row in parallel. The array operates asynchronously, and as long as there are multiplier and multiplicand bits in the X and Y registers, the array will continue to accumulate the partial products.

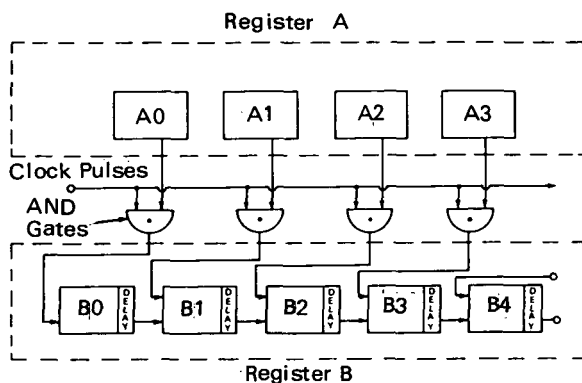
Source: G. Y. Wang  
Electronics Research Center  
(ERC-90076)

Circle 17 on Reader Service Card.

## SIMPLE CIRCUIT PERFORMS BINARY ADDITION AND SUBTRACTION

Binary addition and subtraction are performed with a ripple adder (see fig.) that uses dual-input and delayed-output flip-flops in one register.

The ripple adding circuit adds the contents of registers A and B and places the sum in register B. With a binary "1" stored in a stage of



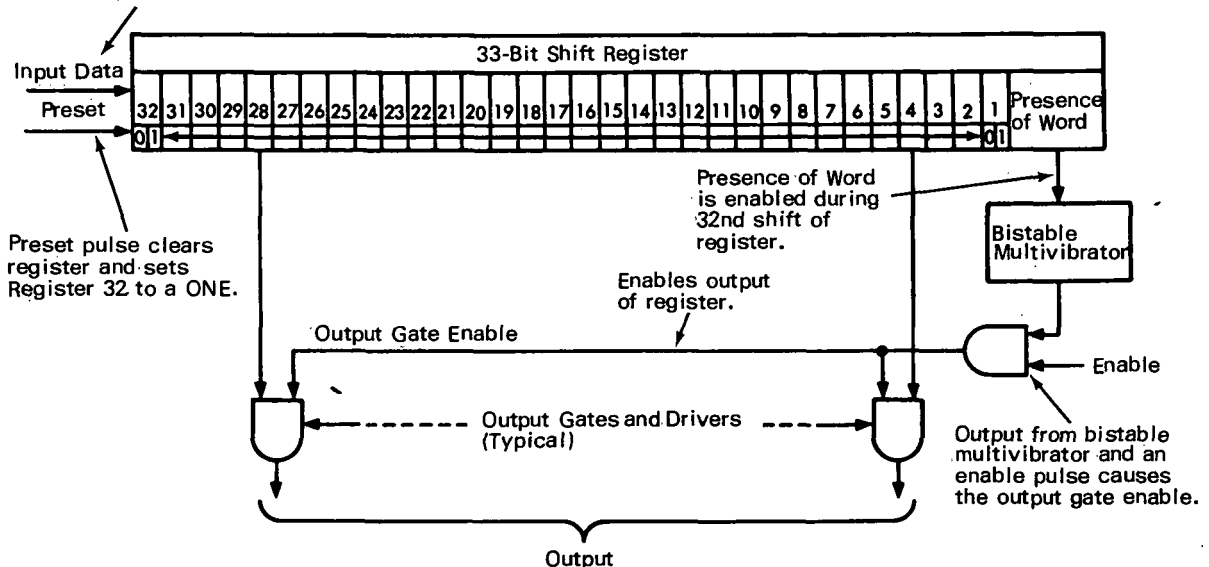
register A, the clock pulse passes through the AND gate corresponding to that stage and triggers the input of the corresponding stage of register B. For addition, register B is designed to give an output pulse on the "1"-to-"0" transition. This output pulse is delayed from the input of the next stage to permit the contents of register A to be transferred before the ripple pulses travel through register B. For subtraction, register B produces an output pulse on the "0"-to-"1" transition, and the circuit subtracts the contents of register A from the contents of register B.

Source: D. H. Schaefer and R. A. Cliff  
Goddard Space Flight Center  
(GSC-00399)

Circle 18 on Reader Service Card.

## OPERATING A 32-BIT DECODER WITHOUT A COUNTER CIRCUIT

Input is applied to register.



A conventional decoder for processing 32-bit word codes normally uses a counter circuit to control the output gate necessary in sequencing the decoded output. The counter circuit, composed of several bistable multivibrators working in parallel with the bit register, is costly and decreases the reliability of the decoder. A novel

decoder circuit using a 33-bit shift register, eliminates the 32-bit counter, and uses an extra bit count to set the register for the next word.

When operating the register without a counter (see fig.), a 33-bit shift register is employed in which a ONE has previously been preset into the highest bit position. The 32-bit serialized input

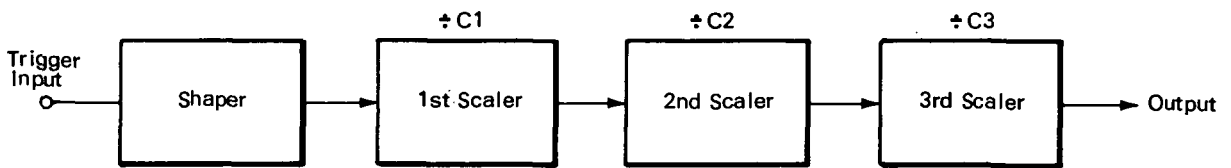
word is fed into the shift register and shifted 32 times. The 33-bit register is simply an addition of one more register circuit to the existing 32-bit register. When the register shifts the 32nd time, the added register, called the presence-of-word register, "enables" the bistable multivibrator. An enabling pulse is "ANDed" with the output pulse of the bistable multivibrator, thus generating the output gate enable which dumps the 32 data bits of the shift register. After the dump occurs, the

circuit is reset with a ONE in the 32nd register, the rest of the register is cleared and now is ready to receive another input word.

Source: G. N. Miller of  
IBM Corp.  
under contract to  
Marshall Space Flight Center  
(MFS-14069)

*Circle 19 on Reader Service Card.*

### MAGNETIC SUBCOUNT CHAIN



Magnetic counting chains which function in a manner similar to flip-flop counters have an important advantage in that they have an extremely low power dissipation factor. This becomes especially significant if the counting chain is long, since the duty cycle of most of the stages would be very low.

In operation, the shaper circuit of the magnetic counting chain buffers an input count signal to provide an output which incrementally saturates a core in the first scaler. After a predetermined number of input pulses to the shaper ( $C1$ ), the core in the first scaler saturates and adds a single count ( $C2$ ) to the second scaler; and after  $C1 \times C2 \times C3$  input counts to the subcount chain, a one-shot pulse is finally generated at the output.

Important advantages offered by this system include: (1) ease of manufacturing; (2) ease of trimming to reduce interface incompatibilities; (3) count flexibility; and (4) ease in extending a counting chain.

Since each electronic module contains a shaper (the shapers are regenerative), no buffering is required between the subcount chains.

Source: H. L. Kasdan, L. S. Jacobs,  
R. G. Radys and F. E. Enright of  
Hughes Aircraft Co.  
under contract to  
Goddard Space Flight Center  
(XGS-11378)

*Circle 20 on Reader Service Card.*

### SELF-CORRECTING, SYNCHRONIZING RING COUNTER USING INTEGRATED CIRCUIT DEVICES

Conventional monitoring techniques require complex circuit configurations and a large number of gate circuits to detect errors which occur when system power is turned on. This error detection and reset logic circuitry uses only three NAND gate circuits.

Figure 1 shows conventional ring counter cir-

cuitry with error detection and reset logic circuitry added (in heavy lines). The necessary initial circuit condition is to have the output of first integrated circuit flip-flop (A) in the logical one condition. When this is so, a preset pulse (P) is simultaneously applied to all flip-flops of the ring counter from NAND gate 3, resulting in any

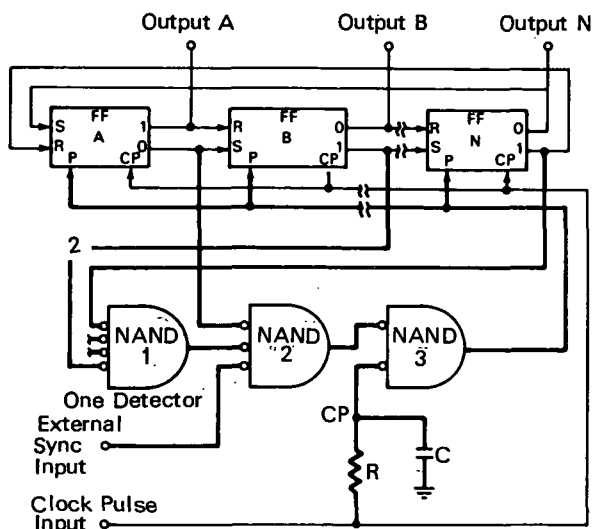


Figure 1. Simplified Diagram

extraneous logical one's being reset to off (i.e., a logical zero state). Thus, the circuit is ready for operation, and the logical one condition of flip-flop A will advance to each successive flip-flop in the loop as the clock pulse (CP) input signals are counted.

By adding a single input to the second NAND gate (2), an external signal may be applied to synchronize the ring counter with another external source.

The CP input is applied to the final gate (3) so that the preset pulse P will not last into the

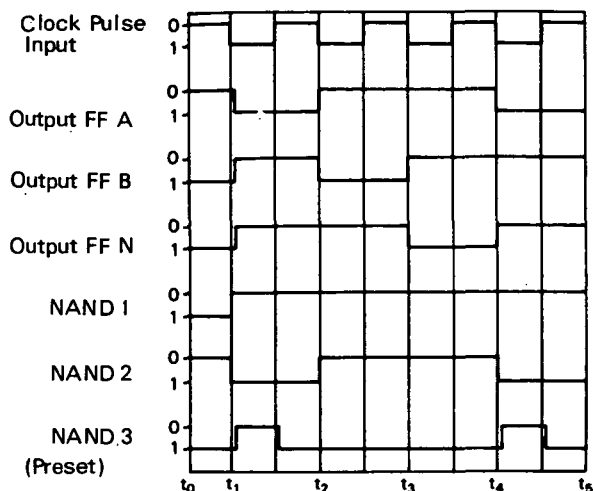


Figure 2. Preset and Timing Signal Sequence of Circuit Using Negative True Logic

following clock time and hold the ring counter in the initial state. The CP input to the last gate is slightly delayed by an RC network so the flip-flops have time to settle before being error-detected.

Source: W. A. Maasberg of  
IBM Corp.

under contract to  
Marshall Space Flight Center  
(MFS-13901)

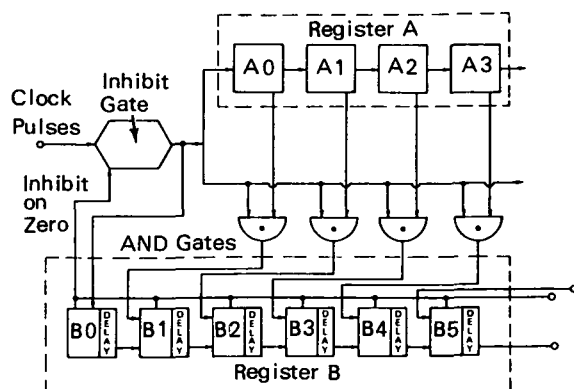
Circle 21 on Reader Service Card.

## DELAYED RIPPLE COUNTER SIMPLIFIES SQUARE-ROOT CALCULATION

This circuit could be combined with small computing device, e.g., a desk top calculator that uses ripple adding counters to provide square-root calculations.

In operation, successively higher numbers are subtracted from the register containing the number from which the square root is to be derived. Using the ripple subtract technique, the last number subtracted is the closest integer to the square root of the number.

Register A, an ordinary counter, is started at zero and after  $n$  clock pulses contains the number  $n$ . Register B, a binary counter, subtracts rather than adds when pulsed. A pulse fed to the first stage of B subtracts 1 from its contents, a



pulse fed to the second stage subtracts 2, a pulse to the third stage subtracts 4, and so on.

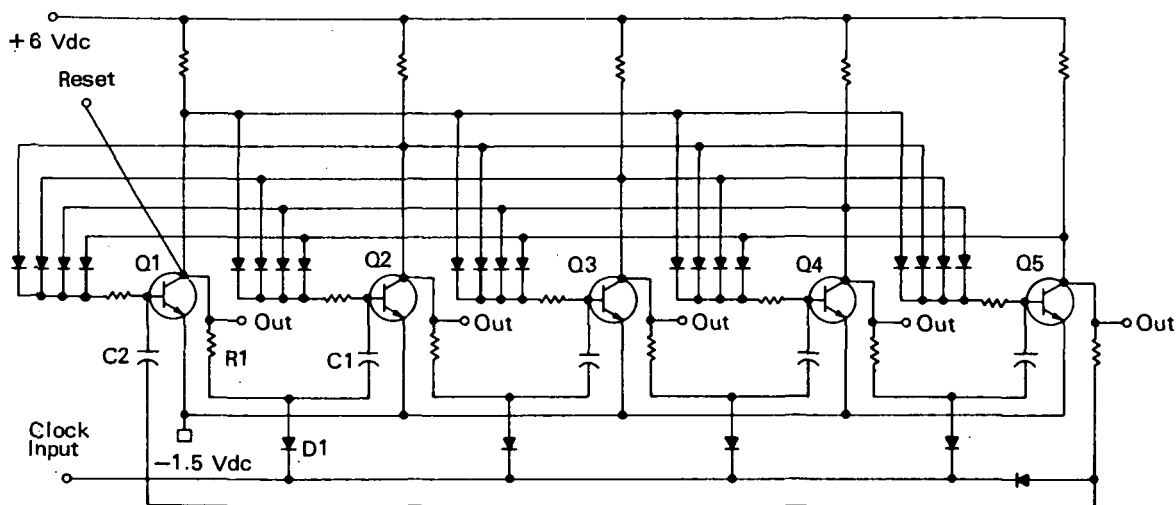
The contents of register A are initially set to zero and the contents of register B, the ripple subtract counter, are set to the number (M). The clock pulses sequentially advance register A and at the same time subtract the contents of each stage of register A containing a "1" from the next stage of register B. When the contents

of register B reach zero or a negative value, the clock pulses are inhibited and the value of the closest integer to the square root of M is read from register A.

Source: R. Cliff  
Goddard Space Flight Center  
(GSC-00398)

*Circle 22 on Reader Service Card.*

### PENTAL CIRCUIT MAY BE USED IN CONVERSIONLESS DECIMAL COUNTER



The pental counter circuit is designed to eliminate the conversion circuitry which must be used when binary circuits are employed to generate or process numeric information. It can be constructed from one pental circuit, one standard flip-flop, and several AND gates.

The counter circuit has five stable states which are triggered sequentially from left to right in synchronism with the input clock pulses. In this condition, when Q1 is off, the other four transistors are in the on state (low collector voltage).

The trailing edge of the clock pulse causes Q2 to be turned off, permitting its collector voltage to rise. The base current of Q2 then maintains Q3, Q4, and Q5 in the on state and also turns Q1 on. On the next clock pulse the trigger circuit,

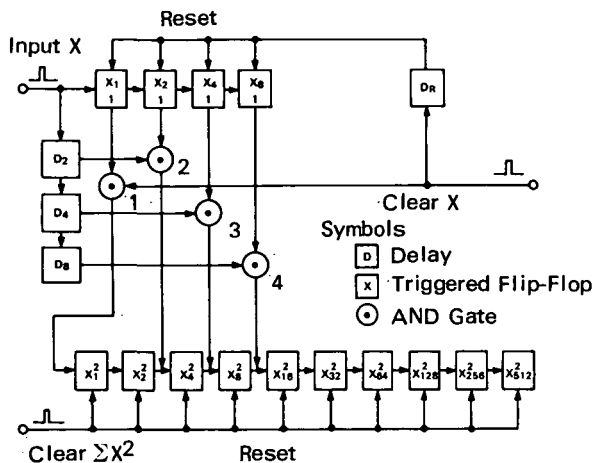
associated with transistor Q2 is fired, and Q3 is turned off. Succeeding pulses step the off position farther to the right. The cycle is completed by connecting capacitor C2 (in the trigger circuit of Q5) to the base of Q1, allowing the sequence to be fed back from Q5 to Q1. The counter may be reset to zero by applying a positive pulse to the collector of Q1 and to the base of the transistor associated with the on state of the flip-flop.

Source: D. H. Galvin, Jr. of  
Massachusetts Institute of Technology  
under contract to  
NASA Headquarters  
(HQN-10146)

*Circle 23 on Reader Service Card.*

## SIMPLE PULSE COUNTING CIRCUIT COMPUTES SUM OF SQUARES

A pulse counting circuit calculates the sum of the squares,  $\Sigma X^2$ , of numbers represented by a series of pulse trains.



The circuit configuration shown in the figure uses 4 flip-flops to count up to 15, and 10 additional flip-flops to store the sum of the squares. The four primary counting flip-flops are reset by a pulse on the clear-X line after each sequence of pulses. At the end of the summation, the 10

summing flip-flops are cleared by a pulse on the clear- $X^2$ .

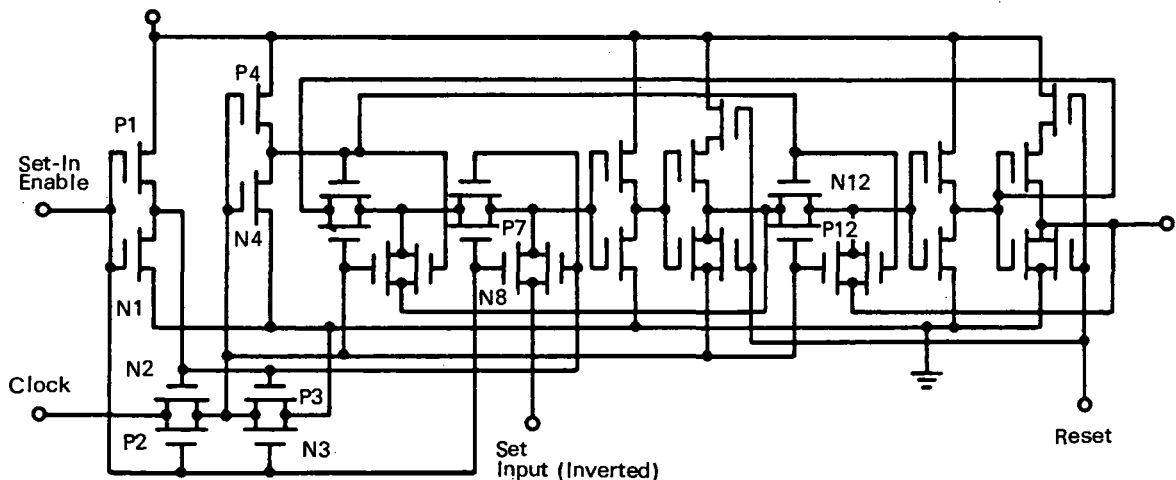
In a typical operation, three sequential pulses arrive at the input terminal. The first pulse turns on flip-flop  $X_1$ ; the second pulse turns  $X_1$  off,  $X_2$  on, and also travels through delay line  $D_2$  to trigger flip-flop  $X_2^2$ . The third pulse, in a similar manner, causes  $X_2^2$  to turn off and  $X_4^2$  to turn on. Before the primary counter is reset, the  $\Sigma X^2$  counter differs from the actual sum of the squares by one if the number of input pulses is odd. This is corrected when the clear-X pulse arrives and triggers the  $X^2$  flip-flop. For an even number of input pulses, the clear-X pulse is not passed through AND gate 1 because flip-flop  $X_1$  is off.

An important advantage of this system is the continuous summation of the squares of the pulses during the completion of the pulse train.

Source: D. H. Schaefer  
Goddard Space Flight Center  
(GSC-00391)

Circle 24 on Reader Service Card.

## COMPLEMENTARY-MOS BINARY COUNTER WITH PARALLEL-SET INPUTS



This circuit, which can be operated at clock rates to 5 MHz, should be useful in computer applications as a special purpose counter with parallel gated inputs and simple data-hold capability.

The MOS four-stage binary counter features a new reset scheme plus four parallel-set inputs gated in by a "set-in enable" signal. Four parallel-set inputs permit setting the counter into any of sixteen possible states.

A basic counter stage shown in the figure consists of two cross-coupled flip-flops that change state on the negative-going edge of the clock signal. The "set-in enable" signal gates-in the set-input information. With the "set-in enable" at +V, the internal clock line (i.e., gates of P4 and N4) assumes ground potential because transmission gate P3-N3 is on. Transmission gate P7-N7 opens, unlocking the first flip-flop and allowing the set-input signal to transfer into the first flip-flop through transmission gate P12-N12 to the output. When the "set-in enable" signal returns to ground, the first or second flip-flop (depending upon whether the clock signal is at ground or +V potential) will be locked and a state change will not occur at the counter state output. This counter circuit maintains its set state after the "set-in enable" signal returns to ground independent of the potential at the clock input.

The following documentation may be obtained from:

National Technical Information Service  
Springfield, Virginia 22151  
Single document price \$3.00  
(or microfiche \$0.95)

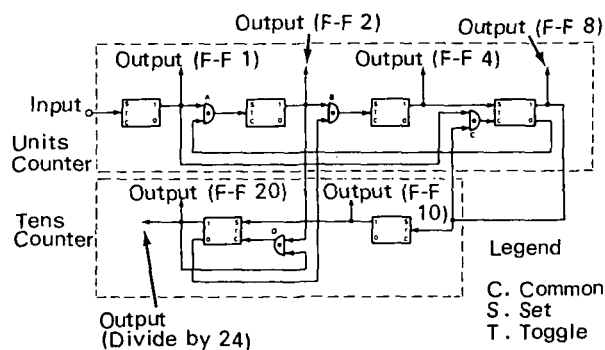
Reference:

NASA-CR-86171 (N69-30472) Design and Development of a Digital Subsystem Employing N- and P-Channel MOSFET's in Complementary Circuits in an Integrated Circuit Array

Source: A. K. Yung and K. R. Keller of  
Radio Corporation of America  
under contract to  
Electronics Research Center  
(ERC-10122)

### SIMPLE BCD CIRCUIT ACCURATELY COUNTS TO 24

This divide-by-24 counter can be used in digital control clocks to register hours and give a daily output signal. The ripple-through counter



requires only 6 modules and generates the final count by means of feedback loops, without producing false output spikes in the transition to the 24th count.

Flip-flops 1, 2, 4, and 8 provide a BCD count to nine in the normal manner. The transition of

flip-flop 8 from the "1" state to the "0" state generates the carry to the following stage. When the 8th pulse is registered, normally closed gate C is opened, and normally open gate A is closed. The 10th pulse, therefore, resets flip-flop 8 but does not set flip-flop 2 as it normally would. The resetting of flip-flop 8 causes flip-flop 10 to be set. The same process occurs when the 20th pulse is encountered, except that flip-flop 10 is reset and flip-flop 20 is set. At the same time, normally open gate B is closed, and normally closed gate D is opened. When the 24th pulse arrives, it resets flip-flop 20 but cannot set flip-flop 4. The 24th pulse, therefore, resets the entire counter and produces the divide-by-24 output pulse.

Source: M. L. Spafford  
Goddard Space Flight Center  
(GSC-00317)

Circle 25 on Reader Service Card.



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